Section 10. Parallel Slave Port

HIGHLIGHTS

This section of the manual contains the following major topics:

10.1 Introduction

Some devices have an 8-bit wide Parallel Slave Port (PSP). This port is multiplexed onto one of the devices I/O ports. The PORT operates as an 8-bit wide Parallel Slave Port, or microprocessor port, when the PSPMODE control bit is set. In this mode, the input buffers are TTL.

In slave mode the module is asynchronously readable and writable by the external world through $\overline{RD}$ control input pin and the $\overline{WR}$ control input pin.

It can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORT latch as an 8-bit latch. Setting the PSPMODE bit enables port pins to be the $\overline{RD}$ input, the $\overline{WR}$ input, and the $\overline{CS}$ (chip select) input.

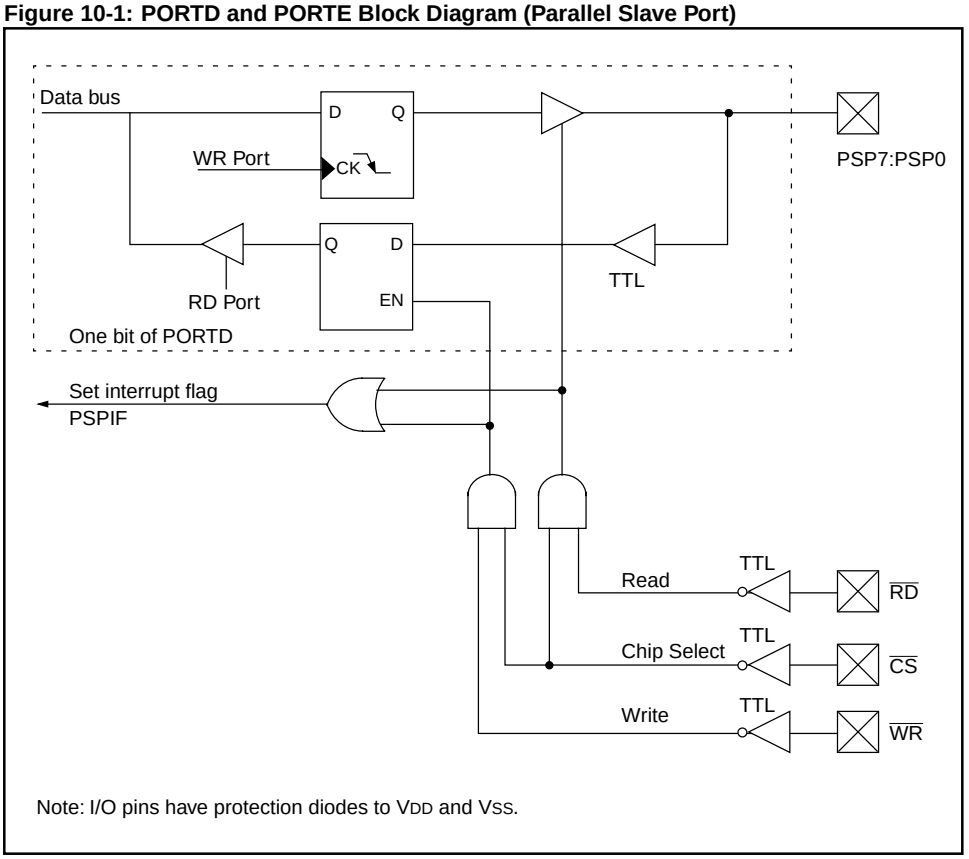
Note 1: At present the Parallel Slave Port (PSP) is only multiplexed onto PORTD and PORTE. The microprocessor port becomes enabled when the PSPMODE bit is set. In this mode, the user must make sure that PORTD and PORTE are configured as digital I/O. That is, peripheral modules multiplexed onto the PSP functions are disabled (such as the A/D).
When PORTE is configured for digital I/O. PORTD will override the values in the TRISD register.

Note 2: In this mode the PORTD and PORTE input buffers are TTL. The control bits for the PSP operation are located in TRISE.

There are actually two 8-bit latches, one for data-out (from the PICmicro) and one for data input. The user writes 8-bit data to PORT data latch and reads data from the port pin latch (note that they have the same address). In this mode, the TRIS register is ignored, since the microprocessor is controlling the direction of data flow.

Figure 10-1 shows the block diagram for the PSP.

Figure 10-1: PORTD and PORTE Block Diagram (Parallel Slave Port)



Note: I/O pins have protection diodes to VDD and VSS.

10.2 Control Register

Register 10-1: TRISE Register

R-0	R-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0
bit 7							bit 0

bit 7 **IBF:** Input Buffer Full Status bit

1 = A word has been received and waiting to be read by the CPU
0 = No word has been received

bit 6 **OBF**: Output Buffer Full Status bit

1 = The output buffer still holds a previously written word
0 = The output buffer has been read

bit 5 **IBOV**: Input Buffer Overflow Detect bit (in microprocessor mode)

1 = A write occurred when a previously input word has not been read (must be cleared in software)

0 = No overflow occurred

bit 4 **PSPMODE**: Parallel Slave Port Mode Select bit

1 = Parallel slave port mode
0 = General purpose I/O mode

bit 3 **Unimplemented:** Read as '0'

bit 2 **TRISE2**: RE2 direction control bit

1 = Input
0 = Output

bit 1 **TRISE1**: RE1 direction control bit

1 = Input
0 = Output

bit 0 **TRISE0**: RE0 direction control bit

1 = Input
0 = Output

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

10.3 Operation

A write to the PSP from the external system, occurs when both the $\overline{CS}$ and $\overline{WR}$ lines are first detected low. When either the $\overline{CS}$ or $\overline{WR}$ lines become high (edge triggered), the Input Buffer Full status flag bit IBF (TRISE<7>) is set on the Q4 clock cycle, following the next Q2 cycle, to signal the write is complete. The interrupt flag bit, PSPIF, is also set on the same Q4 clock cycle. The IBF flag bit is inhibited from being cleared for additional TCY cycles (see parameter 66). If the IBF flag bit is cleared by reading the PORTD input latch, and this has to be a read-only instruction (i.e., MOVF) and not a read-modify-write instruction. The input Buffer Overflow status flag bit IBOV (TRISE<5>) is set if a second write to the Parallel Slave Port is attempted when the previous byte has not been read out of the buffer.

A read from the PSP from the external system, occurs when both the $\overline{CS}$ and $\overline{RD}$ lines are first detected low. The Output Buffer Full status flag bit OBF (TRISE<6>) is cleared immediately indicating that the PORTD latch was read by the external bus. When either the $\overline{CS}$ or $\overline{RD}$ pin becomes high (edge triggered), the interrupt flag bit PSPIF is set on the Q4 clock cycle, following the next Q2 cycle, indicating that the read is complete. OBF remains low until data is written to PORTD by the user firmware.

Input Buffer Full Status Flag bit IBF, is set if a received word is waiting to be read by the CPU. Once the PORT input latch is read, the IBF bit is cleared. The IBF bit is a read only status bit. Output Buffer Full Status Flag bit OBF, is set if a word written to PORT latch is waiting to be read by the external bus. Once the PORTD output latch is read by the microprocessor, OBF is cleared. Input Buffer Overflow Status Flag bit IBOV is set if a second write to the microprocessor port is attempted when the previous word has not been read by the CPU (the first word is retained in the buffer).

When not in Parallel Slave Port mode, the IBF and OBF bits are held clear. However, if flag bit IBOV was previously set, it must be cleared in the software.

An interrupt is generated and latched into flag bit PSPIF when a read or a write operation is completed. Interrupt flag bit PSPIF must be cleared by user software and the interrupt can be disabled by clearing interrupt enable bit PSPIE.

Table 10-1: PORTE Functions

Name	Function
$\overline{RD}$	Read Control Input in parallel slave port mode: $\overline{RD}$ 1 = Not a read operation 0 = Read operation. Reads PORTD register (if chip selected)
$\overline{WR}$	Write Control Input in parallel slave port mode: $\overline{WR}$ 1 = Not a write operation 0 = Write operation. Writes PORTD register (if chip selected)
$\overline{CS}$	Chip Select Control Input in parallel slave port mode: $\overline{CS}$ 1 = Device is not selected 0 = Device is selected

Note: The PSP may have other functions multiplexed onto the same pins. For the PSP to operate, the pins must be configured as digital I/O.

10.4 Operation in Sleep Mode

When in sleep mode the microprocessor may still read and write the Parallel Slave Port. These actions will set the PSPIF bit. If the PSP interrupts are enabled, this will wake the processor from sleep mode so that the PSP data latch may be either read, or written with the next value for the microprocessor.

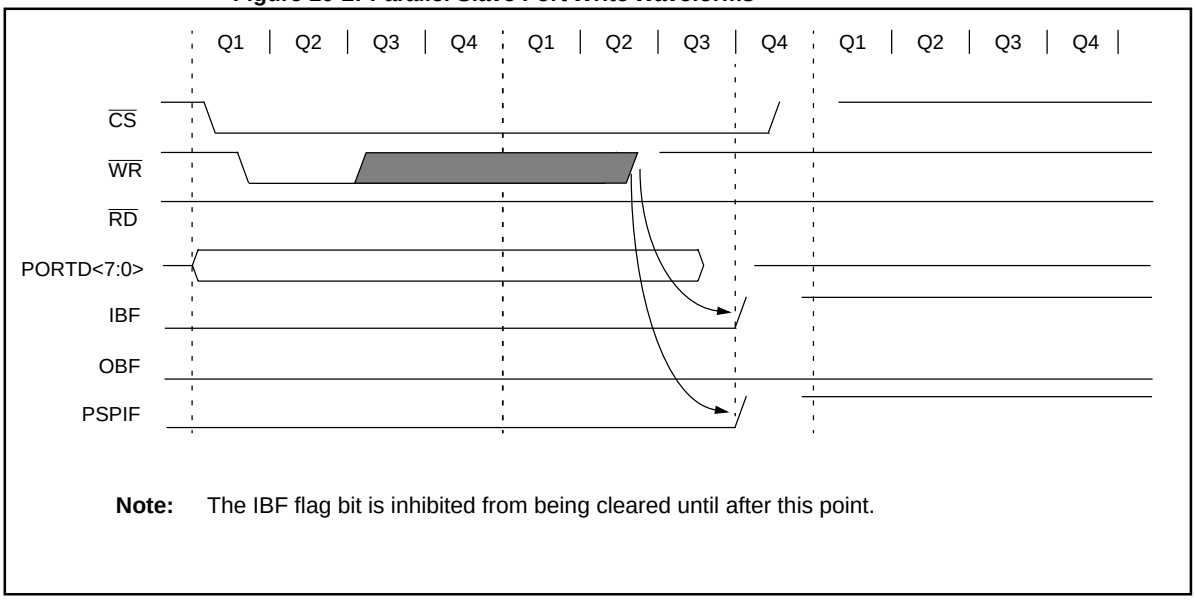
10.5 Effect of a Reset

After any reset the PSP is disabled and PORTD and PORTE are forced to their default mode.

10.6 PSP Waveforms

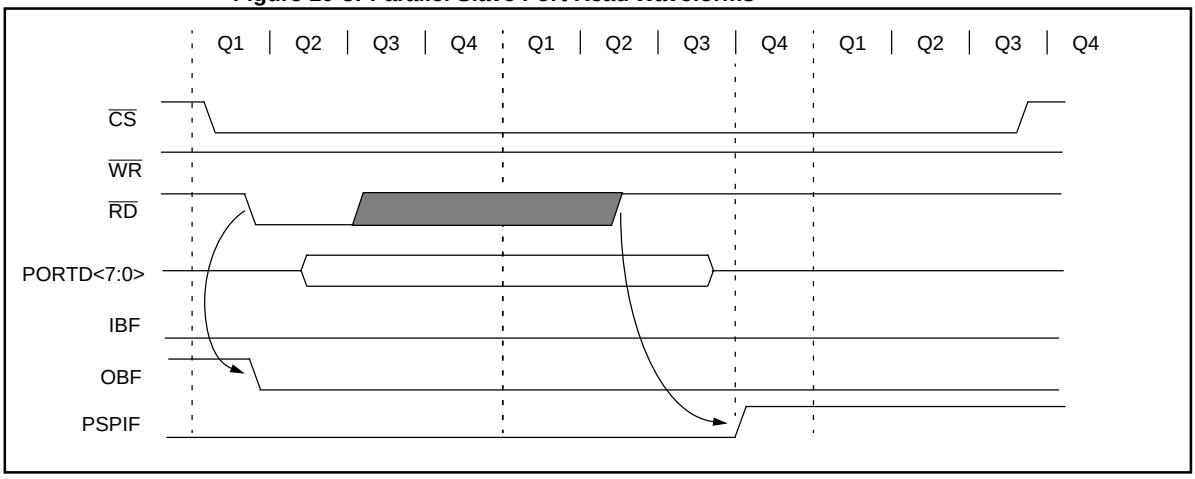
Figure 10-2 shows the waveform for a write from the microprocessor to the PSP, while Figure 10-3 shows the waveform for a read of the PSP by the microprocessor.

Figure 10-2: Parallel Slave Port Write Waveforms



Note: The IBF flag bit is inhibited from being cleared until after this point.

Figure 10-3: Parallel Slave Port Read Waveforms



10.7 Design Tips

Question 1: ***Migrating from the PIC16C74 to the PIC16C74A, the operation of the PSP seems to have changed.***

Answer 1:

Yes, a design change was made so the PIC16C74A is edge sensitive (while the PIC16C74 was level sensitive). See Appendix C.9 for more information.

10.8 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the Mid-Range MCU family (that is they may be written for the Base-Line, or High-End families), but the concepts are pertinent, and could be used (with modification and possible limitations). The current application notes related to the Parallel Slave Port are:

Title	Application Note #
Using the 8-bit Parallel Slave Port	AN579

10.9 Revision History

Revision A

This is the initial released revision of the Parallel Slave Port description.